REMARKS

The independent claims 1, 9, and 16 are amended to recite that the base is constituted of a silicon substrate (supported at page 19, line 18). Claims 4, 12, and 18 are canceled without prejudice to reentry. In response to the Office Action:

[1] The drawings were objected to for not showing every feature recited in the claims, specifically, the plurality of wiring patterns and thin oxidation layer, and a drawing correction was required. The objection and requirement are respectfully traversed.

Claim 1, as exemplified in Figs. 1-2, recites a plurality of wiring patterns 42 electrically connected to the electrode pads 34 and extended from the electrode pads 34 to the surface of the extension portion 20.

The Examiner is invited to note that in Fig. 1(B), the electrode pads 34 are shown by dashed lines indicating that they are below the surface, and they are connected to the external terminals 47 located on both the semiconductor chip 30 and the peripheral extended region 21 (see Fig. 1(A)). This extended region 21 coincides with the upper side of the claimed extension portion 20 (page 22, lines 1-3). The extension portion 20 is recited at page 20, line16.

Therefore, it is believed that Fig. 1(B) does show the claimed feature italicized in the paragraph above. The objection and the requirement for a drawing correction are respectfully traversed for the record on this basis, and withdrawal of the objection and the requirement is requested.

However, if the Examiner thinks it advisable then the Applicant will submit a drawing change re-labeling "21" in Fig. 1(A) to read "21(20)" and adding to Fig. 1(B) a dimensioning arrow similar to that of Fig. a(A), with a reference numeral "21(20)" leading to the arrow.

In regard to the thin oxidation layer, the objection is respectfully traversed on the grounds that (1) this feature is so thin that it is thinner than the thinnest line in a drawing, and is not practical to draft as a separate element and (2) the objection is contrary to the 35 USC § 113,

which states that a drawing shall be furnished "where necessary for the understanding of the subject matter sought to be patented." With respect, the drawing of the part with the thin oxidation layer, and a statement that the thin oxidation layer covers it, provides sufficient understanding. Furthermore, the layer does not appear in the claims and is therefore not "subject matter sought to be patented," so that there is believed to be no requirement for illustration.

[2-3] Claims 1-20 were rejected under §102(e) over Shizuno '022. This rejection is respectfully traversed.

Shizuno was filed on November 28, 2003, and this application was filed on October 31, 2003, before Shizuno, and therefore Shizuno is believed not to be prior art. The Examiner refers to the "earlier effective filing date" of Shizuno, presumably meaning Shizuno's foreign priority date (January 8, 2003). However, this date is believed to be irrelevant. The Examiner is referred to MPEP §2163.03, which begins, "***Reference's Foreign Priority Date ... Cannot Be Used as the 35 U.S.C. 102(e) Reference Date***" (emphasis in original).

Furthermore, the priority date of this application is earlier than its U.S. filing date of October 31, 2003, and the Examiner has acknowledged receipt of the certified copy of the priority document (check box 12.1.1 on page 1 of the Action). Therefore, the earlier date of priority should be applicable in this application.

[4-5] Claims 1-6, 9-13, 16, and 18 were rejected under §103 over Park '259 in view of Tokuda '289. This rejection is respectfully traversed.

Claim 1, as exemplified in Figs. 1-2, recites a silicon substrate constituting a base **12**, a semiconductor chip **30** on the base 12 having a first (upper) main surface **36** with a plurality of electrode pads 34 (Fig. 1(B)), a surface protecting film 35 (Fig. 2) formed on the first main surface 36 such that the electrode pads **34** are exposed, a second (lower) main surface **38** which opposes the first main surface 36, and a plurality of side surfaces **37** (Fig. 2) between the surface

of the surface protecting film **35** and the second main surface 38; an insulating extension portion **20** formed so as to surround the side surfaces of the semiconductor chip 30; a plurality of wiring patterns **42** electrically connected to the electrode pads 34 and extended from the electrode pads 34 to the surface of the extension portion 20; a sealing portion **44** formed on (top of) the wiring patterns 42 such that a part of each of the wiring patterns is exposed; and a plurality of external terminals **47** provided over the wiring patterns in a region including the upper side of the extension portion 20.

The base is now claimed to be of silicon. The advantage of this is as follows: The linear coefficient of expansion of the base will be near to that of the chip. Therefore, thermal stress between the base and the chip is decreased. This also results in greater design freedom as to the pitch and positioning of the external terminals, and a more compact package.

The Examiner is invited to consider:

(1) The Examiner asserts that the heatsink 80 of Park corresponds to the claimed base, but the independent claims recite that a semiconductor chip (claim 1), an extension portion formed from an insulating material (claim 9), or an insulating extension (claim 16), are "on" the base. Park, however, shows that the corresponding features 30 and 50 are *above* the heatsink 80, rather than "on" it. The word "on" is believed to imply contact or closeness of two objects.

To further clarify this distinction, new claims 21-23 recite contact between the corresponding portions and the base (exemplified by contact between features 30 and 12 in Fig. 2, and features 20 and 12 in Figs. 10 and 13).

(2) As noted above, Park's heatsink 80 cannot be a base. Park discloses a "capsule" 50 that corresponds (re claim 1) to the claimed base, because the chip 30 rests on the capsule 50, or alternatively corresponds (re claim 9) to the claimed extension portion with inclined sides, or alternatively corresponds (re claim 16) to the claimed insulating extension portion. Park's capsule is ceramic (col. 3, line 61), not silicon as the Applicant's amended claims recite. Therefore, the capsule 50 cannot anticipate the claimed base.

In Tokuda, the chip 10 rests on a die-attached film 30 which is "adhesive" (col. 10, line 41) and therefore also is not silicon. The substrate 20, on which the film 30 rests, is made of polyimide (col. 10, line 54) and Tokuda gives reasons why this is a preferred material, so there is no teaching toward using another material, such as silicon. In fact, Tokuda mentions silicon but only as having a thermal coefficient that should be matched by the polyimide; thus, while recognizing the problem mentioned by the Applicant above, the solution is different. This teaches against the instant claims.

Thus, neither Park nor Tokuda discloses the claimed silicon substrate. Therefore, no combination of these references (not admitted obvious) could reach the instant claims.

(3) Tokuda is concerned with closely setting chips onto a single surface, and Park is concerned with stacking chips, which is a different object. The Examiner asserts that combination would have been obvious because inexpensively connect wires and pads as taught by Tokuda at col. 3, line 18. However, Park is not concerned with expense, but with signal paths (col. 2, line 31) and clearances (col. 2, line 36), and the rejection presents no reasoned argument as to why or how the expense of Park would be reduced. Fig. 2D of Tokuda shows a process that would not work in the deep ceramic capsule of Park. Tokuda's prior-art Fig. 7A resembles Parks' package, but Tokuda teaches against such a structure at col. 2, line 12 *ff.* The Applicant sees no expectation of success and no motivation for combining the references.

[6] Claims 7, 8, 14, 15, 19, and 20 were rejected under §103 over Park in view of Tokuda and Yamaguchi JP '354. This rejection is respectfully traversed. The Examiner is taking Official Notice of the features of these claims, because the subject matter is not actually disclosed by Yamaguchi, which is respectfully submitted to be irrelevant to these claims. Notice is traversed and the Applicant requests that a reference be cited.

The motivation presented for combining the references is respectfully traversed, as Park and Tokuda are not concerned with high positioning accuracy, as noted above.

[7-8] Claims 1-4 and 6-20 were rejected over the claims of 10/722,446 for obviousness-type double patenting. This rejection is respectfully traversed. The Examiner asserts that the instant claims are broader than the reference claims. However, the instant claims now recite a silicon base, which is not recited in the reference claims, so this statement can no longer be true, even if it were true before (not admitted).

The reference's claim 1 recites a base that is "capable of conducting heat [from the chip] into the atmosphere," while in the instant claims the base is recited to include silicon, and is not claimed to be in contact with the atmosphere.

The question of obviousness is believed to be this: Is a silicon base *per se* obvious over a base "capable of conducting heat ... into the atmosphere"? It is respectfully submitted that the person of ordinary skill would chose a metal for this purpose, not a semiconductor which is inferior to metal in heat conduction. (In fact, the reference's specification teaches in favor of metal in the last sentence of ¶[0118], but the disclosure is not applicable in this sort of rejection, under MPEP §804(B)(1). If it were, however, it would teach against the rejection.)

The reference 10/722,446 was filed on November 28, 2003, after this application was filed, so MPEP §804(B)(1)(b) applies. However, the Examiner has not indicated that the questions of administrative delay and the possibility of the Applicant filing simultaneously with Shizuno were considered.

[9] Claims 1-4 and 6-20 were rejected over the claims of 10/697,247 for obviousness-type double patenting. This rejection is respectfully traversed.

The instant claims all include the feature of a silicon base, while one dependent claim of the reference application recites only a base (dependent claim 3). Conversely, the claims of the reference application all include the feature that "wherein a portions of said wiring patterns on a boundary and vicinity thereof between said semiconductor chip and the extension portion are formed wider or more thickly than other portions of said wiring patterns," which is lacking from

the instant claims. Therefore, the subject matter coverage of this application and the reference are not the same. The Examiner's statement that the instant claims are broader than the claims of the reference is respectfully disagreed with.

Under MPEP §804(B)(1)(a), the question is one-way obviousness because of the filing dates. The question is, are the instant claims obvious over the claims of the reference? That is, would a person of only ordinary skill in the art, considering just the claims of the reference and nothing more, add a *silicon* base? With respect, the Examiner has not established this. The rejection is based solely on one patent being broader than another, which is believed to be incorrect, and there is no argument presented to support one-way obviousness.

Withdrawal of the objections and rejections is requested.

Respectfully submitted,

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